



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

KIMURA et al

Atty. Ref.: 1035-471

Serial No. 10/670,194

Group: 1632

Filed: September 26, 2003

Examiner:

For: CHIP-STACK SEMICONDUCTOR DEVICE AND
MANUFACTURING METHOD OF THE SAME

* * * * *

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

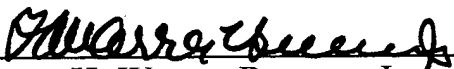
Sir:

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Further to applicants' Information Disclosure Statement of September 26, 2003, applicants herewith submit a corrected Form PTO-1449 (i.e., the number of the first JP reference has been corrected).

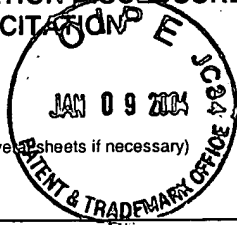
Respectfully submitted,
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January 9, 2004

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**INFORMATION DISCLOSURE
CITATION**



(Use several sheets if necessary)

ATTY. DOCKET NO.

1035-471
APPLICANT

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FILING DATE

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GROUP

1632

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO
223833/1998	08/1998	JAPAN		ABSTR.		
3186941	05/2001	JAPAN		ABSTR.		

OTHER DOCUMENTS (including Author, Title, Date, Pertinent pages, etc.)

*Examiner _____ Date Considered _____

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.